

QUASI RESONANT CURRENT MODE CONTROLLER FOR FLYBACK SWITCHING MODE POWER SUPPLY

1. Description

The iP7500 is a PWM controller with advanced energy features to meet stringent world-wide energy efficiency requirements.

iP7500 combines a true current mode modulator and a zero current detector to ensure full borderline/critical conduction mode in any load/line conditions and minimum drain voltage switching (Quasi-Resonant operation).

Quasi-Resonant operation is achieved by means of a transformer zero current sensing input ZCD that triggers MOSFET on.

The iP7500 integrates built-in advanced energy saving features with high level protection features to provide cost effective and reliable solutions for energy efficient power supplies.

The iP7500 also features an efficient protective circuitry which, in presence of an over-current condition, disables the output pulses and enters a safe mode, trying to restart. Once the fault has gone, the device auto-recovers.

The PWM controller includes, Under-Voltage Lockout (UVLO), Leading Edge Blanking (LEB), optimized gate driver, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with discrete MOSFET and PWM controller solution, the iP7500 can reduce total cost, component count, size and weight ; while simultaneously increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for cost-effective designs of quasi-resonant switching fly back converters.

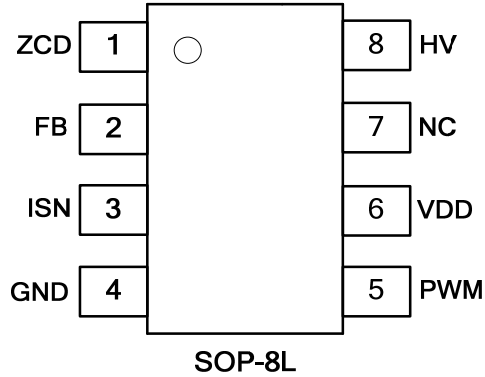
2. Features

- Single-end, pulse by pulse peak current mode PWM
- Quasi resonant for high efficiency and low EMI
- UVLO with high voltage start-up input for fast start-up and low standby current
- Wide operation voltage with OVP latched at 28 V on VDD
- Leading-Edge Blanking (LEB)
- Output soft drive with voltage clamp at 18 V
- Primary current limit, overload and open feedback protection latched
- Auto-recovery on through UVLO crossover
- Reduced current PFM at light load for ultimate power saving
- SOP-8L packaging, with few external components needed
- Internal over temperature protection (OTP) with hysteretic
- Direct opt coupler connection
- Internal minimum turn off time

3. Applications

- Standby SMPS (LCD 、 TV 、 etc.)
- Offline battery chargers (cell phone etc.)
- LED driver (AC-DC LED Lighting.)
- Adapters (Note book, etc.)
- Auxiliary power supplies (DVD players, set-top boxes, LCD TVS, etc.)

4. Pin Assignments



5. Marking Information

Product Name	Marking
iP7500	<div style="border: 1px solid black; padding: 2px; display: inline-block;">iP7500 XXXXX</div> X : Date Code

6. Ordering Code

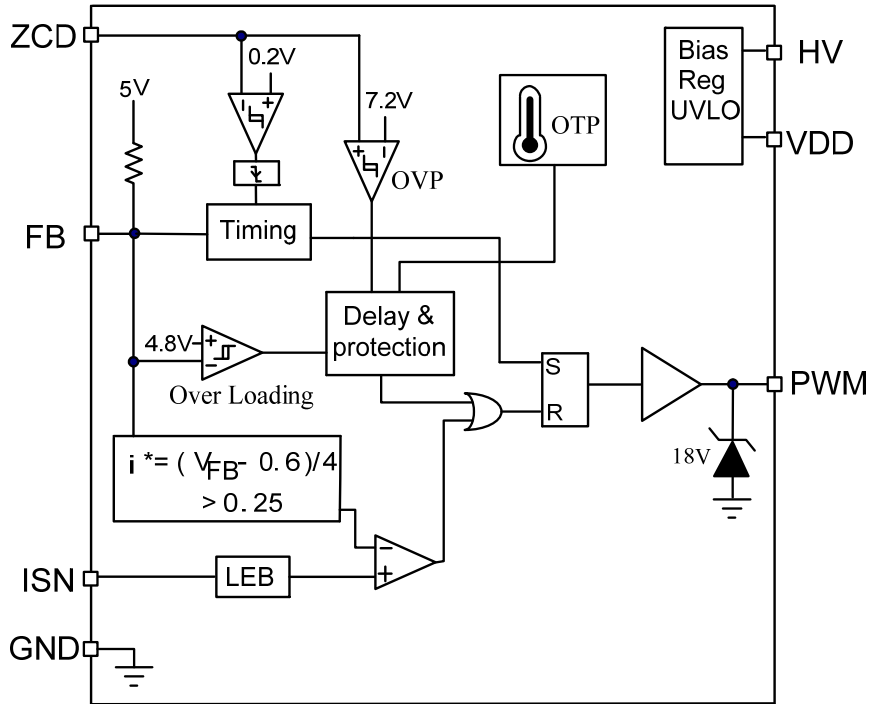
iP7500 <input type="checkbox"/> <input type="checkbox"/> Assembly Material	Assembly Material G: Halogen and Lead Free Device
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Note: inergy defines "Green" as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight ; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

7. Pin Definitions

Pin	Name	Description
1	ZCD	Zero current detect and secondary over voltage protect
2	FB	Feedback in
3	ISN	Current sense
4	GND	Ground
5	PWM	Output PWM
6	VDD	Supply power
7	NC	Non connect
8	HV	High voltage start-up power

8. Block Diagram



9. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	VDD	30	V
Maximum voltage on FB, ISN	-	- 0.3 ~ 6.5	V
Maximum voltage on HV	-	500	V
Maximum voltage on PWM	-	30	V
Maximum junction temperature	T _{Jmax}	150	°C
Storage temperature range	-	- 60 to + 150	°C
Operating junction temperature	T _J	- 40 to + 125	°C
ESD capability, HBM model (All pins except HV)	-	2.0	kV
ESD capability, machine model	-	200	V
Maximum voltage on ZCD	-	VDD + 0.3 ~ VDD - 50	V

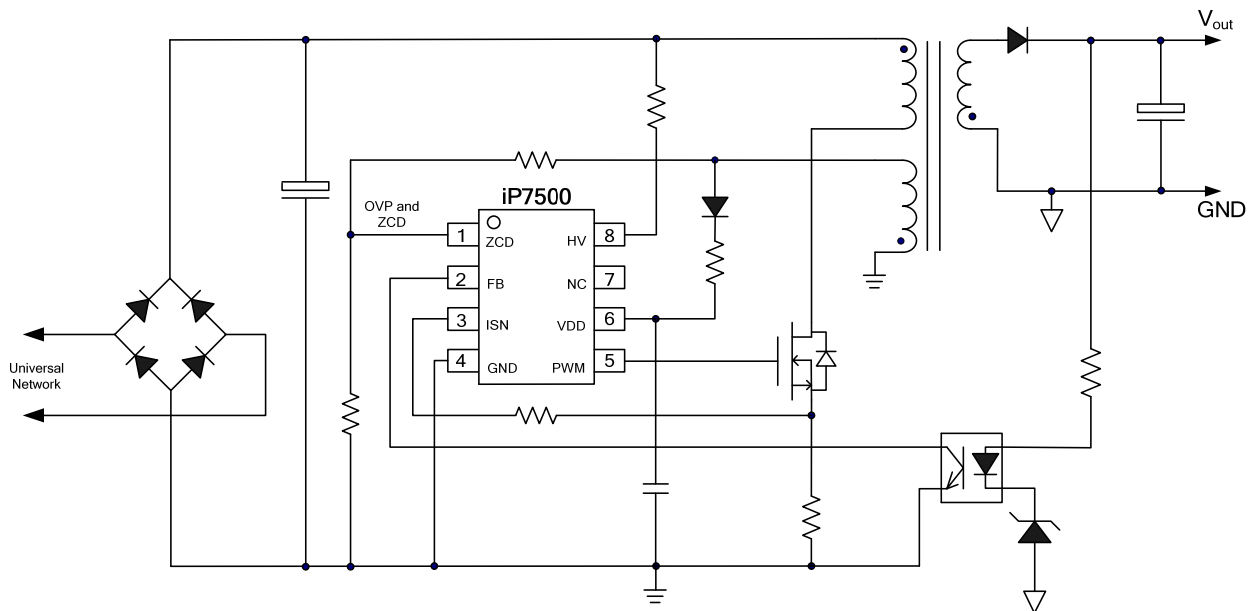
10. Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage section						
Start up current	I_{DDst}		-	20	30	μA
Turn on threshold	V_{DDon}		13	14	15	V
Operating current	I_{DDop}	PWM no load	-	1	1.5	mA
Output off threshold	V_{DDoff}		8	9	10	V
On/off hysteresis	Hys		4	5	6	V
Latched off current	I_{latch}		-	200	-	μA
Latched off clear	$V_{DDlatch}$		-	6	-	V
HV start-up supply section						
HV supply current	$I_{H_{on}}$	$V_{DD} = V_{DDon}$	-	1	-	mA
HV standby current	$I_{H_{stb}}$		-	4	-	μA
Zero Current detect section						
Zero current detect	V_{th}	Negative slope	-	0.2	-	V
Zero current detect hysteresis	V_h		-	0.05	-	V
ZCD input impedance	R_{int}	$< 0 V \text{ or } > 1 V$	-	100	-	$k\Omega$
		$0V < V_{ZCD} < 1$	1	-	-	$M\Omega$
Delay to turn on	t_{zCD}		-	300	-	ns
Input capacitance	C_{par}	$V_{ZCD} = 1.0V$	-	10	-	pF
Minimum off time	t_{OFF}		-	4	-	μs
Secondary OVP threshold	V_{ovth}		-	7.2	-	V
Secondary OVP LEB	t_{sample}		-	2	-	μs
Feedback section						
Pull up resistor	R_{up}		-	20	-	$k\Omega$
Voltage to current	I_{ratio}	$(FB-0.6) / 4$	-	4	-	V/A
FB for PFM onset	V_{PFM}		-	2.6	-	V
Isense section						
Delay to turn off	t_{delay}		-	100	-	ns
LEB	t_{LEB}		-	300	-	ns
High current Limit	V_{ilimit}		-	1.1	-	V
Low current Limit	$V_{illimit}$	PFM mode	-	0.25	-	V
Source current	I_s	Pin open protect	-	1	-	μA

10. Electrical Characteristics (cont.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Protection section						
Over current limit	V_{oc}		-	1.1	-	V
Overload on	V_{ol}		4.5	4.8	5.1	V
Overload delay	t_{od}		-	60	-	ms
Over voltage	V_{ov}	latch	-	28	-	V
Over temp on	T_{ot}		-	125	-	°C
Over temp release	T_{otr}		-	70	-	°C
Output section						
Output rise time	t_{or}	VDD=14 V, CL=1nF	-	320	-	ns
Output fall time	t_{of}	VDD=14 V, CL=1nF	-	60	-	ns

11. Application Circuit



12. Functional Description

iP7500 is a quasi resonant controller for single-end fly back converter. It is designed for AC/DC converter using only minimal external component.

a. Under voltage lock out

The power is supplied between VDD (pin 6) and GND (Pin 4). Below UVLO's on voltage, controller is in UVLO state, it takes very small current as low as 20 uA to detect external voltage and protection means. Pin 6 is supposed to be connected to power in. When VDD below 6 V, an internal HV transistor is turned-on so supply current flows from pin 6 to VDD. When voltage rises above UVLO's on voltage (14V), the controller starts to operate and the HV transistor is turned off. The start-up current is about 4 mA. In the operation mode, controller consumes about 1 mA. It will continue to operate unless the voltage drops below UVLO off voltage (9V), however, the HV transistor will not return on unless VDD voltage drops below 6 V. Between this period, IC consumes 200 uA, so VDD will eventually decrease to 6 V and HV transistor is re-turned-on

b. Feed back

At UVLO, FB pin is sink low with 1 mA current. Once the UVLO is released, V_{FB} is pull up to internal 5 V through a 20 k Ω resistor.

V_{FB} minus 0.6 V and divided by 4 is equal to the reference turn-off current, i^* . So V_{FB} equal to 5 V corresponds to the maxima shunt voltage of current of 1.1 V.

Above half load, V_{FB} of 2.6 V, switching frequency is limited through a 5uSec minimum off-time. Below half-load point, $V_{FB} = 2.6$ V, switching frequency is reduced by increasing the minimum off-time. At quarter-load point, $V_{FB} = 1.6$ V, the minimum off-time is 50 us, corresponds to audible limit 20 kHz. At this load-range, both turn-off peak current and minimum off-time vary.

Below this point, as the load decreases further, V_{FB} is even further down and minimum off time further increases, however, the shunt voltage of turn-off peak current is limited at 0.25 V. Therefore, at light load, V_{FB} controls the output power through the re-turn-on time or minimum off time, resulting to a pure PFM.

Virtually at $V_{FB} = 0.6$ V will correspond to infinite minimum off-time.

If the feedback voltage is higher than 4.9 V for more than 60 ms, PWM will be stopped and latched, which is defined as overload protect. It stays latched till it enters UVLO state.

c. Zero Current detect

The ZCD signal is sensed through an internal resistor of 100 k Ω , and the sensing end is clamped between 0 and 1 V. This voltage is compared with 0.2 V reference, and the falling edge of the comparator's output is used as a set signal for PWM-on. However, the set signal is inhibited for minimum off-time, which is predetermined by feedback voltage.

At full load, PWM will turn-on 300 ns after falling edge of the ZCD signal, which should correspond to the 1st valley of MOSFET's drain voltage. A small capacitor may be connected between ZCD and ground to delay the turn-on time to match the valley's minima. As the load decreases, the MOSFET's drain voltage falling edge comes sooner. At some point, the 1st falling edge comes sooner than minimum off-time, so set signal is masked and turn-on is not initiated, then drain voltage will continue to oscillate, but with decreasing amplitude. The next falling edge which comes after minimum off-time will generate turn-on signal to trigger on PWM.

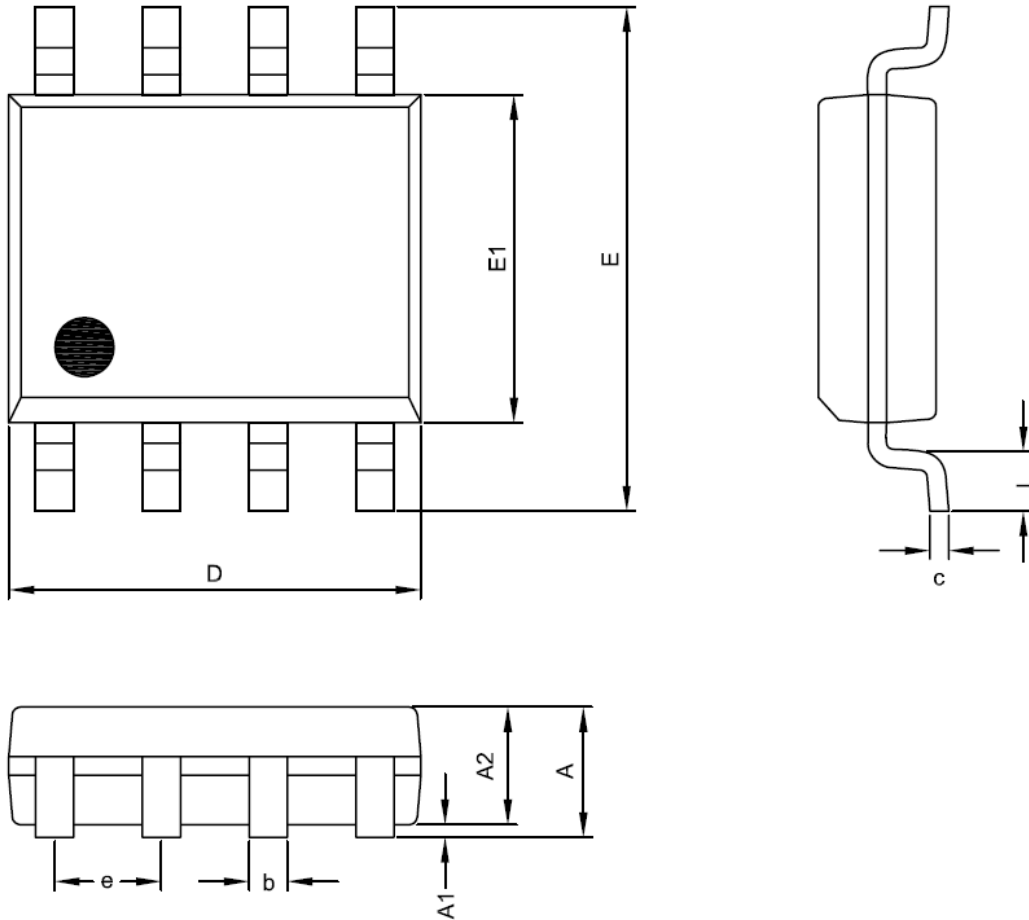
d. Current sense

ZCD signal triggers PWM to turn-on main MOSFET, and current through transformer primary winding and MOSFET starts to increase. This current is monitored through ISN pin, which senses the voltage across the shunt resistor. When the current reaches reference turn-off current, i^* , the MOSFET is turn-off.

Very often, even though it is not prominent at quasi-resonant converter, at MOSFET turn-on is a current spike caused by the discharge of parasitic capacitance of MOSFET and diode. So in here a 300 ns mask for not to detect the current sensing (Leading edge blanking/LEB) is included to prevent premature turn-off.

13. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.